**IN THE CLAIMS:**

1. (Currently Amended) A system comprising:

a source device;

a destination device coupled to the source device;

wherein the source device is configured to violate a known communications rule, and wherein the destination device is configured to detect said violating a known communications rule, and wherein the destination device includes a phase locked loop (PLL);

wherein said violating a known communications rule indicates to the destination device a change in the state of the system, and wherein said violating comprises the source device driving a clock signal to the destination device at a frequency that is outside of a specified frequency range, and wherein the PLL is configured to detect said driving a clock signal outside of the specified frequency range.

2. (Original) The system as recited in claim 1, wherein said violating indicates a command from the source device to the destination device to change the state of the system.

3. (Original) The system as recited in claim 1, wherein said violating provides an indication from the source device to the destination device that a change in the state of the system has occurred.

4. Cancelled.

5. Cancelled.

6. Cancelled

7. Cancelled.

8. Cancelled.

9. (Original) The system as recited in claim 1, wherein said violating comprises driving signals from an input pin of the source device, and wherein the destination device is configured to detect said driving.

10. (Original) The system as recited in claim 1, wherein the system is a computer system, the computer system comprising:
a processor;
an input/output (I/O) controller coupled to the processor;
a peripheral bus coupled to the I/O controller; and
at least one peripheral device coupled to the peripheral bus.

11. (Original) The system as recited in claim 10, wherein the computer system comprises a docking station and a mobile unit.

12. (Original) The system as recited in claim 11, wherein said violating indicates that the mobile unit is to be undocked from the docking station.

13. (Original) The system as recited in claim 10, wherein the peripheral device is a plug-and-play peripheral device.

14. (Original) The system as recited in claim 13, wherein said violating indicates that the peripheral device is to be removed from the system.

15. (Original) The system as recited in claim 13, wherein said violating indicates that the peripheral device has been inserted into the system.

16. (Original) The system as recited in claim 10, wherein said violating indicates that the peripheral device has been inactive for a predetermined period of time.

17. (Currently Amended) A method comprising:
a source device communicating with a destination device;
the source device violating a known communications rule;
the destination device detecting said violating, wherein said detecting indicates to the destination device a change of state of a system comprising the source device and the destination device, and
detecting said violating with a phase-locked loop (PLL), wherein the PLL is comprised by the destination device, wherein said violating comprises the source device driving a clock signal to the destination device at a frequency that is outside of a specified frequency range, and wherein the PLL is configured to detect said driving a clock signal outside of the specified frequency range.

18. (Original) The method as recited in claim 17, wherein said violating indicates a command from the source device to the destination device to change the state of the system.

19. (Original) The method as recited in claim 17, wherein said violating provides an indication from the source device to the destination device that a change in the state of the system has occurred.

20. Cancelled.

21. Cancelled.

22. Cancelled.

23. Cancelled.

24. Cancelled.

25. (Original) The method as recited in claim 17, wherein said violating comprises driving signals from an input pin of the source device, wherein the destination device is configured to detect said driving.

26. (Original) The method as recited in claim 17, wherein the system comprising the source device and the destination device is a computer system, the computer system comprising:
a processor;
an input/output (I/O) controller coupled to the processor;
a peripheral bus coupled to the I/O controller; and
at least on peripheral device coupled to the peripheral bus.

27. (Original) The method as recited in claim 26, wherein the computer system comprises a docking station and a mobile unit.

28. (Original) The method as recited in claim 27, wherein said violating indicates that the mobile unit is to be undocked from the docking station.

29. (Original) The method as recited in claim 26, wherein the peripheral device is a plug-and-play peripheral device.

30. (Original) The method as recited in claim 29, wherein said violating indicates that the peripheral device is to be removed from the system.

31. (Original) The method as recited in claim 29, wherein said violating indicates that the peripheral device has been inserted into the system.

32. (Original) The method as recited in claim 26, wherein said violating indicates that the peripheral device has been inactive for a predetermined period of time.

33. (New) A system comprising:

a source device;

a destination device coupled to the source device;

wherein the source device is configured to violate a known communications rule, and wherein the destination device is configured to detect said violating a known communications rule, and wherein the destination device includes a phase locked loop (PLL);

wherein said violating comprises the source device changing the frequency of a clock signal by a specified amount, wherein the PLL is configured to detect said violating by detecting said changing the frequency.

34. (New) A system comprising

a source device;

a destination device coupled to the source device;

wherein the source device is configured to violate a known communications rule, and wherein the destination device is configured to detect said violating a known communications rule, and wherein the destination device includes a phase locked loop (PLL), and wherein said violating comprises the source device transmitting a frequency modulated signal to the destination device, and wherein the destination device is configured to detect the frequency modulated signal.

35. (New) A system comprising:

a source device;

a destination device coupled to the source device;

wherein the source device is configured to violate a known communications rule, and wherein the destination device is configured to detect said violating a known communications rule;

wherein said violating a known communications rule indicates to the destination device a change in the state of the system, and wherein said violating comprises the source device transmitting a combination of clock signals and data signals to the destination device, wherein the combination is in violation of a standard encoding.